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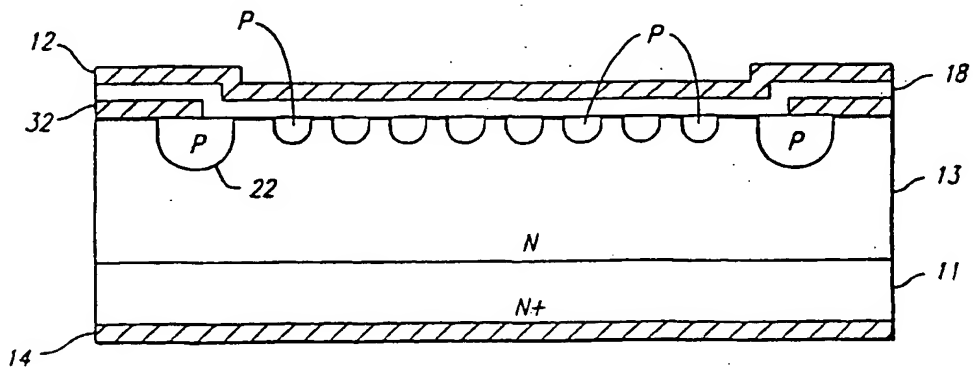
(54) Title: DISCRETE SCHOTTKY DIODE DEVICE WITH REDUCED LEAKAGE CURRENT



(57) Abstract: A discrete Schottky diode device employing a vertical device structure with current flow between the top and bottom major surfaces of the discrete device. The device employs a large number of commonly connected Schottky barrier regions (18) interspersed with strips of reverse current blocking regions (P). These blocking regions are doped with an opposite conductivity type to the semiconductor substrate in the Schottky barrier regions. Application of a reverse voltage to the device causes the depletion zones from adjacent blocking strips to merge, blocking reverse leakage current. By suitable selection of geometry, spacing and doping of the blocking regions effective blocking of reverse current leakage is provided.

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DISCRETE SCHOTTKY DIODE DEVICE WITH REDUCED LEAKAGE CURRENT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to discrete semiconductor devices. More specifically, the present invention relates to discrete diode devices and Schottky diode devices in particular.

2. Background of the Invention

Discrete diodes have a wide variety of applications including applications in power supplies, voltage converters and clamping circuits. For example, such applications are found in personal computers and other electronic devices and systems. In such applications, it is important to provide both a fast recovery time for the diode and a low forward voltage drop across the diode (V_f). For example, a fast recovery time is needed for rectification of high frequency signals which are present in computers and many other electronic devices. Also, such signals in current computers operate at low voltages, for example, 1-3 volts.

Semiconductor junction diodes are the most common diodes due to their reliability and relatively low cost, due to well developed semiconductor manufacturing techniques. Nonetheless, semiconductor junction diodes may not provide the desired characteristics for some applications, particularly high speed/low voltage applications. While it is possible to adjust the properties of the diode junction to increase the recovery speed of the semiconductor diode or to reduce the V_f of the diode, it is typically impossible to simultaneously lower both the voltage drop across the diode and at the same time decrease the recovery time of the diode. This presents a problem and the compromise is usually made in favor of fast recovery times.

Schottky diodes provide advantages over semiconductor junction diodes since Schottky diodes have a lower V_f for a given recovery time than semiconductor diodes. Nonetheless, existing Schottky diodes suffer from problems such as high leakage current and reverse power dissipation. Also, these problems increase with temperature causing reliability problems for applications, such as power supplies, which require operation at higher temperatures. Therefore, the design of systems such as power supplies and voltage converters using Schottky barrier diodes can cause design problems for many applications.

In view of the foregoing, it will be appreciated that existing Schottky diodes fail to provide all the desirable characteristics needed for demanding applications. Therefore, a need presently exists for an improved Schottky diode having more controllable device characteristics, especially reduced leakage current. Furthermore, it will be appreciated that a need presently exists for such a device which is not unduly complex and which is readily compatible with available integrated circuit processing techniques and which may be produced at low cost.

SUMMARY OF THE INVENTION

The present invention provides an improved Schottky diode device having reduced leakage current and reduced reverse power dissipation. The present invention further provides a method for manufacturing such a Schottky diode which is compatible with existing semiconductor technology, which provides a high degree of reliability in device characteristics and which can provide such devices at reduced cost.

In a preferred embodiment, the present invention provides a discrete Schottky diode device employing a vertical device structure, i.e., with current flow between the top and bottom major surfaces of the discrete device. The device employs a large number of commonly connected Schottky barrier regions interspersed with strips of reverse current blocking regions. These blocking

regions are doped with an opposite conductivity type to the semiconductor substrate in the Schottky barrier regions. Application of a reverse voltage to the device causes the depletion zones from adjacent blocking strips to merge, blocking reverse leakage current. By suitable selection of geometry, spacing and doping of the blocking regions the active area of the device may be reduced by a relatively small amount, while providing effective blocking of reverse current leakage.

In a further aspect, the present invention provides a method of fabricating an improved discrete Schottky diode device employing relatively few masking steps and relatively low cost. The method employs forming a large number of closely spaced blocking regions on a semiconductor substrate via masking, implantation and diffusion (RTP) steps employing conventional semiconductor processing techniques. A Schottky metal is deposited over the active surface to form a Schottky barrier with the underlying substrate. Electrical contact metallization layers are then formed on the top and bottom surfaces of the substrate, to create a vertical device structure with a current flow path between the top and bottom surfaces. Only one additional masking step is required over conventional Schottky formation processes allowing the significant improvements in device performance to be achieved with moderate cost increase. In an alternative embodiment of the present invention, the number of masking steps may be reduced by replacing conventional guard ring structures and associated masking step with structures to reduce electric fields adjacent chip pin outs which are defined by existing masking steps.

Further features and advantages of the present invention will be appreciated by review of the following detailed description of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A is a top view of a portion of the Schottky diode device of the present invention.

Figure 1B is a side sectional view of a portion of the Schottky diode device shown in Figure 1A.

Figure 1C is a side sectional view of the entire Schottky diode device structure.

Figure 2A-2C are schematic drawings of the operation of the Schottky diode of the present invention.

Figures 3A-3F are side schematic drawings illustrating one method of fabricating the Schottky diode device illustrated in Figures 1A-1C.

Figures 4A and 4B are side sectional and top views, respectively, of an edge portion of the integrated circuit chip of the Schottky diode device of the present invention illustrating the guard ring structure adjacent the contact pads.

Figures 5A-5F are side sectional schematic drawings illustrating an alternate method of fabricating a Schottky diode device in accordance with the present invention.

Figures 6A-6F are side sectional schematic drawings illustrating another alternate method of fabricating a Schottky diode device in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to Figures 1A-1C, the structure of the improved Schottky diode device 10 of the present invention is illustrated in top and two side sectional views, respectively. The Schottky diode device of the present invention is a discrete vertical device with current flowing between the bottom and top major surfaces of the integrated circuit to provide the desired current capacity needed

for applications such as circuit clamps and rectifying applications such as in voltage converters and power supplies. The Schottky diode device is a two-terminal device and the current flow is thus between a first contact 12 configured on the top surface of the integrated circuit substrate 11 (shown in Figures 1B and 1C) and a second contact 14 configured on the bottom surface of the substrate. The substrate is composed of a semiconductor material, preferably silicon. Other materials, such as GaAs, may also be employed, however.

The Schottky diode device 10 includes a plurality of commonly connected Schottky metal barrier regions 16 which cover a majority of the top surface of the substrate (e.g., 80% or more). The regions 16 are preferably formed in an epitaxial layer 13 of the substrate situated above a more heavily doped portion 11 of the semiconductor substrate. The regions 16 comprise a layer of metal 18, of a type suitable for forming a Schottky barrier with the semiconductor material of the substrate as known in the art. The metal layer 18 is in direct contact with the substrate in each region 16 so as to form a Schottky barrier. For example, nicel, titanium, platinum, molybdenum and palladium form suitable Schottky barrier junctions with silicon and may be employed for metal layer 18. Interspersed with the Schottky barrier regions 16 are reverse current blocking regions 20. Preferably a large number of regions 16, 20 are provided, e.g., up to 10 thousand - 100 thousand per cm at crossection. Both regions 20 and 16 are preferably elongated strips having relatively narrow width dimensions d_1, d_2, respectively, and an elongated length dimension. For example, the length dimension of the regions 16, 20 may extend over all or a substantial portion of the top surface of the integrated circuit chip comprising a discrete device. It will be appreciated, however, that alternate geometries may be employed, including various shaped interdigitated regions or other geometries of interspersed regions 16, 20. In any case, it is desirable to minimize the dimension d_1 to minimize the surface area occupied by the blocking regions 20 and maximize the current carrying area; for example, in accordance with a presently preferred embodiment of the device 10 the dimension d_1 may be on the order of 0.2-0.5 microns. In

general, the distance d_2 between blocking regions will be significantly greater than d_1, for example, about 10 times d_1. Therefore, d_2 may be about 2-5 microns in a presently preferred embodiment. These dimensions are not shown to scale in the drawings, for convenience of illustration.

As may be best appreciated from Figure1C, the device 10 preferably also includes guard ring 22 which protect against breakdown where the device pin-outs connect to the contact 12. These may be conventional in design. Alternative breakdown prevention structures in accordance with several embodiments are discussed below. Oxide regions 32 partially overlap the guard rings 22 and define the boundaries of the active area of the device.

A variety of modifications may be made to the device 10, while remaining within the scope of the present invention. For example, as noted above, alternate geometries of regions 16 and/or 20 may be provided. Also, although the device 10 is illustrated as an N type device it may also be provided as a P type device and the appropriate N to P substitutions are to be understood in the Figures for such a P type embodiment. Also, GaAs may be employed as the substrate with metal layer 18 chosen to form a Schottky barrier with GaAs.

Referring to Figures 2A-2C, the operation of the blocking regions 20 in blocking undesirable reverse leakage currents in the Schottky diode device of the present invention is illustrated.

In Figure 2A, the device 10 is illustrated in a forward biased (or an unbiased) mode showing the blocking regions 20 having depletion regions 24. The depletion regions 24 have a size determined by the concentrations of the dopant in the P type blocking regions 20 and in the N type substrate 13. These concentrations are chosen, based on the spacing d_2, such that the depletion regions 24 of adjacent blocking regions are spaced apart during normal forward biased operation of the diode. For most applications, the concentration of the N type substrate will be chosen for the desired Schottky barrier height to optimize the speed and V_f for the particular application and the P type dopant concentration in blocking regions 20 will be chosen to provide the desired

depletion region size. Typically, such concentrations will be chosen in the range of about 10^{16} - 10^{21} cm^{-3} for the blocking regions 20 to provide the desired depletion region size for spacings d_2 between blocking regions of 0.2-0.5 microns.

In Figure 2B, the device 10 is illustrated as a reverse bias begins to be applied to the diode. As shown, the depletion regions 24 around blocking regions 20 expand to begin to pinch off the N type substrate.

Finally, in Figure 2C the device 10 is illustrated with a full reverse bias voltage applied to the diode, corresponding to normal operation of the device. As shown the depletion regions have merged with substantially all the majority carriers depleted from the Schottky barrier regions 16. As a result reverse leakage current through these regions is completely blocked.

Accordingly, it will be appreciated that the present invention provides a Schottky diode device which is not subject to the detrimental reverse leakage current characteristics of known Schottky diodes and which is simple in structure and which is readily manufactured in a cost effective manner. Although some active surface area of the device is lost to the blocking regions 20, nonetheless, this lost area can be minimized by using low area geometries, such as long narrow strips, with a dopant concentration tailored to the spacing of the strips. In addition, lower work function barrier metals can be used instead of the high barrier metals since according to this invention the barrier metal does not determine the reverse leakage. Such a choice may lead to an overall lower Vf. As a result, the Schottky diode device of the present invention maintains the desirable features of Schottky diodes, i.e., speed and low on resistance, while avoiding reverse leakage current problems. Also, the device is easy to manufacture and has a high degree of reliability in its electrical characteristics despite inevitable process variations. Further advantages of the device 10 will be appreciated from the discussion below of a preferred method of manufacture thereof.

Referring to Figures 3A-3F, the process flow for a preferred embodiment of method of manufacturing a Schottky diode device in accordance with the present invention is illustrated in a series of schematic sectional drawings. Figures 3A-3E illustrate a portion of the wafer as it is processed, the illustrated portion generally corresponding to a small portion of a single device as illustrated in Figures 1A-1C. It will of course be appreciated that in practice the structure as shown in the figures is repeated many times over the surface of the wafer for each dye and in which multiple dyes are processed together.

Referring first to Figure 3A, an epitaxial region 13 is formed on a substrate 11 in a conventional manner. The process flow will be illustrated for an N channel device and, accordingly, the epitaxial region 13 is shown as N type having, for example, As concentrations in the range of 10^{14} - 10^{16} cm^{-3}. If a P type device is desired, the dopant will be P type instead of N type and it is to be understood herein that all such doped regions may simply be reversed from N to P type and P to N type to create a P type device and such is implied for each of the following process steps.

An optional N type region 15 of higher concentration may also be provided to tailor the barrier height of the Schottky barrier regions. Region 15 may be implanted to increase the dopant concentration levels or increased dopants may be introduced during the final growth of the epitaxial layer 13 to provide the desired increased concentration levels. For convenience of illustration the region 15 will be suppressed in the remaining drawings but it is to be understood that in appropriate cases, the layer 15 may be present as an upper layer of epitaxial region 13.

Referring to Figure 3B, guard ring regions 22 are formed on the surface of the epitaxial layer 13. These regions 22 may be formed in a conventional manner, employing a mask layer 30 which is exposed and etched to open the areas for implanting the guard rings regions, e.g., with a P type dopant as shown. Alternate methods for forming guard regions will be described below.

Referring to Figure 3C, the process flow proceeds with a masking step to open the active area of the device. This stage of the process includes removal of photoresist 30, depositing a new photoresist mask layer and exposing the mask layer to define the active region 34. This is followed by growth of an SiO_2 layer 32 outside of the active region. The photoresist over region 34 is then removed, leaving oxide layer 32. These masking, exposure, oxidation and mask removal acts may be conventional in nature.

Referring to Figure 3D, the next stage of the process of the present invention is illustrated. In Figure 3D only a portion of the active area 34 of the device is shown in order to better illustrate the process flow. As shown, a photoresistive mask layer 36 is deposited, exposed and etched to provide openings 38 for defining blocking regions 20. A dopant, e.g., a P type dopant such as boron is then implanted through the openings 38 as illustrated. To control the width of regions 20, a shallow implant followed by a thermal diffusion / activation of the dopant may be employed to control the final depth and width of regions 20. The mask layer 36 is then removed. Since it is desirable to keep these doped layers as shallow as possible (in particular, in order to minimize the influence of the parasitic J-FET), the preferred method of impurity activation can be Rapid Thermal Processing (RTP).

Next, the process flow of the present invention proceeds to the deposition of a Schottky barrier metal layer 18 as illustrated in Figure 3E. Metallization layer 18 is chosen to provide the desired Schottky barrier voltage with the semiconductor substrate; for example, it may be composed of well-known metals, such as molybdenum, aluminum, platinum, palladium, etc. or a combination of metals chosen to provide the desired barrier height with silicon as is known in the art. The deposition of the Schottky barrier metal layer 28 is followed by a thermal processing step, for example, a rapid thermal processing step, to form the Schottky barrier.

The process flow then proceeds to deposit a TiNi layer or other barrier layer over the layer 28 and proceeds with conventional metallization and

passivation steps. This is followed by a chip metallization masking and deposition step, thinning of the substrate 11 and formation of the source contact 12 and 14. The wafer is diced to result in a separate Schottky diode device as illustrated in Figure 3F.

It will be appreciated by those skilled in the art that the above process flow provides significant advantages in the quality of the Schottky devices formed thereby and can therefore improve yield, and hence reduce cost of the devices made thereby. Although the described process flow requires four masking steps, i.e., for formation of the guard ring regions 22, formation of the active regions, formation of the blocking regions and for the chip metallization, i.e., an additional step over conventional processes for discrete Schottky diodes, this may be offset by increases in yield. Further advantages of the above-described process will be appreciated by those skilled in the art.

Referring to Figures 4A and 4B, one implementation of guard rings 22 is illustrated. The region of the integrated circuit illustrated in Figures 4A and 4B corresponds to an edge portion of the integrated circuit.

More specifically, referring to Figure 4B, an annular shaped guard ring 22 is formed. For example, the guard ring 22 may be a round, square or rectangular annular shape. The guard ring 22 for example, may be from about 3-10 microns along one side of the guard ring, with, for example, about five microns being presently preferred. The guard ring 22 is preferably formed of a relatively deep P- region 40 in the case of N type doped epi - layers active devices (or N- region in the case of P type doped epi-layers active devices). For example, a boron implant of about 10^{15} - 10^{16} cm^{-3} with a depth of about 2,000-10,000 Å may be employed. A shallower P+ contact region 42 is formed on top of the P- region 40 to provide good ohmic contact with the metallization layer. For example, the P+ contact region 42 may comprise a boron implant with a concentration of about 10^{18}- 10^{19} cm^{-3}.

The guard ring implants 40 and 42 preferably abut against the Schottky barrier regions 16. In this way, the relatively diffuse region 40 provides a low

field blocking junction with the epitaxial region 13 adjacent the edge portion of the integrated circuit chip, which region is most susceptible to breakdown. Accordingly, it will be appreciated that the guard ring structure illustrated in Figures 4A and 4B reduces undesired breakdown of the Schottky diode device of the present invention.

Referring to Figures 5A-5F an alternative embodiment of the Schottky diode device and method of making same in accordance with the present invention is illustrated. In the case of Figures 5A-5F the illustrations are cross-sectional portions of a wafer showing the Schottky diode device at various stages of the process flow.

Specifically referring to Figure 5A, the initial stage is illustrated for a small portion of the wafer with a semiconductor substrate being provided having an epitaxial region 13 formed on a more heavily lower doped portion of the substrate 11. The substrate is illustrated as doped N type, but a P type substrate may also be employed and appropriate dopant substitutions are to be understood throughout the Figures for such an alternate embodiment.

Referring to Figure 5B, the process flow proceeds to define the blocking regions 20 through a masking layer 36 which is deposited and opened as in the case of the previously described process flow in relation to Figure 3D above. The regions 20 are then implanted through the openings in the masking layer 36 and diffused, through a thermal diffusion step, to precisely define the desired depth, width and concentration level of the blocking regions 20.

Referring to Figure 5C, the next stage in the process flow corresponds generally to the Schottky barrier metal deposition step described above in relation to Figure 3E and includes deposition of Schottky metal layer 18, directly on the top surface of the substrate, followed by a thermal processing step, for example, a RTP step, to form the Schottky barrier with the underlying substrate in the Schottky barrier regions 16. Unlike the previously described process flow in relation to Figure 3E, however, the process flow in Figure 5C is not proceeded by a masking step to define active areas of the device and rather the entire top

surface of the substrate is deposited with the Schottky metal 18. Also, a separate masking step to define guard ring regions is not provided prior to the process flow of Figure 5C. Therefore, it will be appreciated that two masking steps have been eliminated from the prior described process flow.

Referring to Figure 5D, the process flow is illustrated after conventional deposition of contact layer 12 on top of the Schottky metal layer 18. As also shown in Figure 5D, a second conductive contact 14 is deposited on the bottom surface of the substrate 11 after thinning of the substrate. As further illustrated in Figure 5D, dicing lanes 50 have been etched in the upper surface of the substrate to define the individual dies which will constitute the separate discrete diode devices 10. Such formation of dicing lanes 15 may be in a conventional manner as known to those skilled in the art. For convenience of illustration the number of blocking regions and Schottky regions 16 shown does not reflect the actual number in the device which, as noted above, will typically be a relatively large number of such regions, for example 1 - 100 million cm^{-2}.

Referring to Figure 5E, the next stage in the process flow is illustrated. As shown, an oxide layer 52 is deposited over the top surface of the entire wafer including the sides and bottom of the open dicing lanes 50. This oxide layer 52 may be grown using any of a number of known processes.

Finally, referring to Figure 5F, the process flow is illustrated after the oxide layer 52 has been anisotropically etched to leave residual side oxide regions 54 on the edge portions of the active surface area of each device 10. The side oxide structures 54 reduce the electric field in the area of the edge of the chip and provide an effective alternative to conventional guard rings to prevent breakdown operation of the device through high electrical fields in this region. As illustrated in Figure 5F, the diode device 10 has been separated from neighboring devices by dicing of the wafer to leave a single integrated circuit. As in the previous illustrations, only a fraction of the total number of blocking regions and Schottky barrier regions are illustrated. Also, the Figures greatly exaggerate

the dimension of the blocking regions 20, to better illustrate the structure of the device.

Accordingly, it should be appreciated that the method illustrated in Figures 5A-5F provides a Schottky device 10 which has desirable characteristics such as those described previously and which may be manufactured using only two masking stages in the process flow. Since each masking stage adds cost to the process, it will be appreciated that the method illustrated has advantages in cost reductions over previously described embodiments.

It should also be appreciated that the process flow illustrated in Figures 5A-5F may also be employed to fabricate a conventional Schottky diode device excluding reverse current blocking regions 20 by simply eliminating the masking step illustrated in Figure 5D. This would result in a conventional Schottky diode device fabricated using a single masking step and having the side wall oxide structures 54 in place of conventional guard ring structures for breakdown protection. This would result in a one-step process as compared to two steps employed in the prior art resulting in significant cost advantages. This Schottky diode device may be preferred where the reverse blocking regions 20 are not necessary for controlling leakage currents for the particular application of the Schottky diode device.

Referring to Figures 6A-6G, an alternate embodiment of the Schottky diode device and method of making same is illustrated. As in the case of the previously described embodiments for manufacturing Schottky diode devices, the process flow is illustrated in a series of stages, the drawings corresponding to sectional views through portions of a wafer. For convenience of illustration, the various regions are not shown to scale.

Referring to Figure 6A, the process flow includes a stage of providing a semiconductor substrate having an epitaxial layer 13 on top of a more heavily doped underlying substrate 11 as in the previously described embodiments.

Referring to Figure 6B, the process flow proceeds to provide an oxide layer 60 on top of the epitaxial area 13. Layer 60 may cover the entire wafer.

Growth of the oxide layer 60 may be done in a conventional manner as is well known to those skilled in the art.

Referring to Figure 6C, the next stage in the process flow includes providing an open area 62 corresponding to the active region of an individual device. This stage includes a first masking step to deposit photo-resistive mask layer 64 followed by a mask removal etch to expose open area 62 corresponding to the active region of the device.

Referring to Figure 6D, the process flow proceeds to the next stage wherein a selective SiO_2 etch is performed to remove the oxide in the open area 62 corresponding to the active region of the device. This etch will partially etch the oxide underlying the photoresistive mask layer 64, as shown. Such a selective oxide etch may be performed using conventional etching techniques well known to those skilled in the art, for example a HF wet etch may be employed. The residual mask layer 64 is then removed.

Referring to Figure 6E, the process flow proceeds to the next stage wherein a second masking step is employed to deposit a masking layer 66 to define the blocking regions 20. Exposure of the mask layer 66 is followed by etching the mask layer to open an area 68 over each of the blocking regions 20. This is followed by a P implant as illustrated and a thermal diffusion of the dopant, to provide the desired depth, width and concentration of the blocking regions 20. Due to the presence of the sloped sidewall of the oxide layer 60, tapered doping concentrations will be provided for the P type dopant deposited in these regions. These tapered P type implanted regions 70 adjacent to the edge portions of the active region 62 will reduce electric fields and may thus effectively operate as breakdown prevention regions in place of more conventional guard ring structures such as described in the first described embodiment.

Referring to Figure 6F, the process flow of the present invention includes deposition of a Schottky metal layer 18 on top of the substrate followed by RTP to create the Schottky barrier with the underlying substrate.

Referring to Figure 6G, the process flow proceeds with thinning of the substrate and deposition of top and bottom contacts 12 and 14, respectively. Also, it will be understood that conventional passivation, metallization and dicing steps may be provided as is well-known in the art. The illustrated process flow thus provides a breakdown barrier region at the edge of the device as in the first described embodiment of the present invention while avoiding an additional masking step. This modified process for forming breakdown prevention regions 70 may also be employed to form otherwise conventional Schottky diodes by omitting the formation of barrier regions 20. Accordingly, it will be appreciated that in some applications the illustrated approach may be more cost-effective than the earlier described embodiment.

Accordingly, it will be appreciated that the present invention provides several embodiments of a Schottky diode device and methods of manufacture of Schottky diode devices which provide significant advantages over the prior art. In particular, such advantages include low leakage current while retaining low on resistance, low forward voltage V_f, and fast recovery time. Also, good reliability in the electrical characteristics of the device and hence good yield are provided.

Furthermore, it should be appreciated that the above-described description of the preferred embodiment is merely illustrative in nature and a variety of modifications to both the device structure and the process flow may be provided while remaining within the scope of the present invention. Also, it should be appreciated that features or advantages of the preferred embodiments or other aspects of the described embodiments, are not to be deemed critical or essential to the present invention unless so stated.

What Is Claimed Is:

1. A Schottky diode device, comprising:

a semiconductor substrate doped with a first dopant of a first conductivity type and having a first major surface and a second major surface;

a plurality of Schottky barrier regions on the first major surface;

a plurality of blocking regions of a second dopant of a second conductivity type on the first major surface interspersed with the Schottky barrier regions; and

first and second electrical contacts on the first and second major surfaces, respectively, which define a current flow path between the major surfaces through the plurality of Schottky barrier regions.

2. A diode device as set out in claim 1, wherein each Schottky barrier region comprises a Schottky metal layer in direct contact with said semiconductor substrate.

3. A diode device as set out in claim 1, wherein said blocking regions are elongated strips.

4. A diode device as set out in claim 3, wherein said Schottky barrier regions are elongated strips alternating with said blocking region strips.

5. A diode device as set out in claim 4, wherein said Schottky barrier region strips are about ten times the width of said blocking region strips.

6. A rectifier device as set out in claim 1, wherein said first dopant is an N type dopant and wherein said second dopant is a P type dopant.

7. A diode device as set out in claim 2, wherein said Schottky metal is composed of Ti, molybdenum, aluminum, platinum, palladium , silicides of molybdenum, aluminum, platinum, or any other known metals or their silicide capable of forming a Schottky barrier with Si.

8. A diode device as set out in claim 6, wherein said blocking region is doped to about 10^{16} - 10^{21} cm^{-3} of a P type dopant.

9. A diode device as set out in claim 3, wherein said blocking regions have a width of about 0.2-0.5 microns.

10. A Schottky diode device, comprising:

a semiconductor substrate having first and second surfaces and having a plurality of Schottky barrier regions on the first surface, a first contact electrically connected to the Schottky barrier regions and a second contact on the second surface; and

a plurality of blocking means, configured adjacent each Schottky barrier region, for blocking current flow between said first and second contacts in response to a reverse bias voltage applied to said diode device.

11. A diode device as set out in claim 10, wherein each Schottky barrier region comprises a Schottky metal layer in direct contact with said semiconductor substrate.

12. A diode device as set out in claim 11, wherein said Schottky barrier regions are configured as a plurality of parallel elongated strips.

13. A diode device as set out in claim 11, wherein the blocking means comprise narrow strips of dopant implanted in said substrate adjacent said Schottky barrier regions.

14. A method of fabricating a Schottky diode device, comprising the steps of:

providing a semiconductor substrate doped with a first conductivity type dopant and having a top and bottom surface;

forming a plurality of blocking regions in said substrate;

forming a plurality of Schottky barrier regions; and

forming first and second electrical contact layers on said top and bottom surfaces, respectively, to provide a current flow path between said surfaces., respectively, to provide a current flow path between said surfaces.

15. A method as set out in claim 14, wherein forming a plurality of blocking regions comprises implanting a dopant of a second conductivity type in narrow strips into said substrate.

16. A method as set out in claim 15, wherein the dopant concentration formed by said implanting is about 10^{16} - 10^{21} cm^{-3}.

17. A method as in claim 15, wherein said first dopant is arsenic and said second dopant is boron.

18. A method as set out in claim 14, wherein forming said Schottky barrier regions comprises depositing a layer of a metal on said semiconductor substrate.

19. A method as in claim 18, wherein said metal is molybdenum, aluminum, platinum, or palladium.

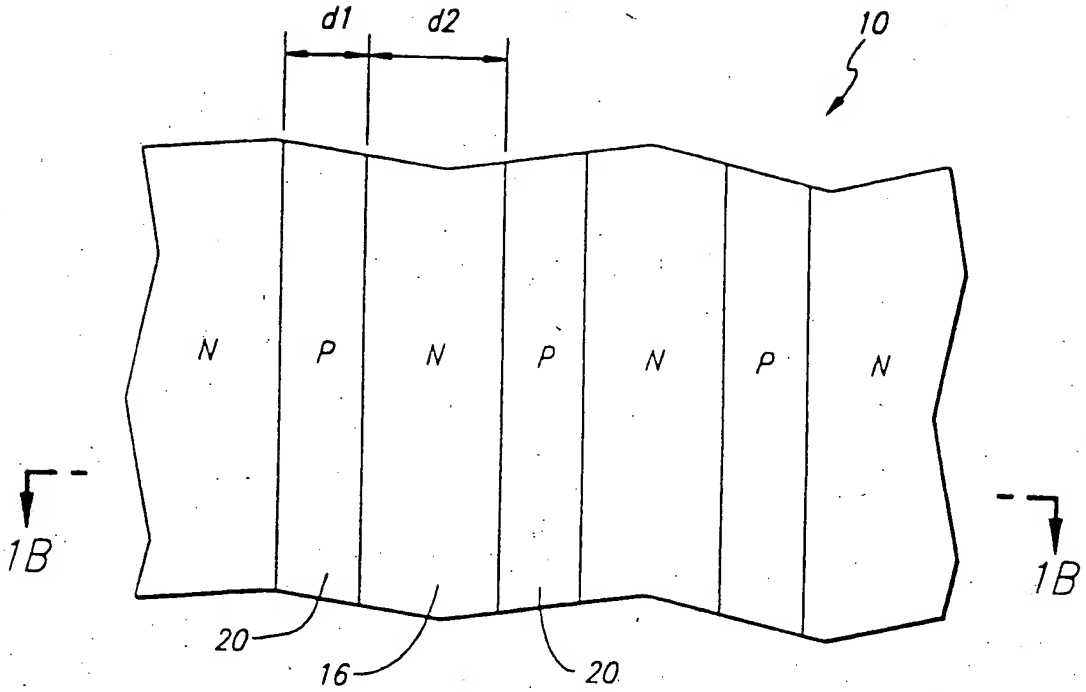
20. A method as set out in claim 14, further comprising, prior to forming said blocking regions, forming a plurality of plug implants and guard ring implants of said first conductivity type in respective plug and guard ring regions.

21. A method as set out in claim 20, wherein said plug and guard ring implant steps provide peak concentrations of about 10^{15} - 10^{16} cm^{-3}.

22. A method as in claim 20, wherein a single masking step is employed to form said plug and guard ring regions.

23. A method as set out in claim 21, wherein said plug and guard ring implant steps further comprise a shallow implant of about 10^{17} - 10^{19} cm^{-3}.

FIG. 1A



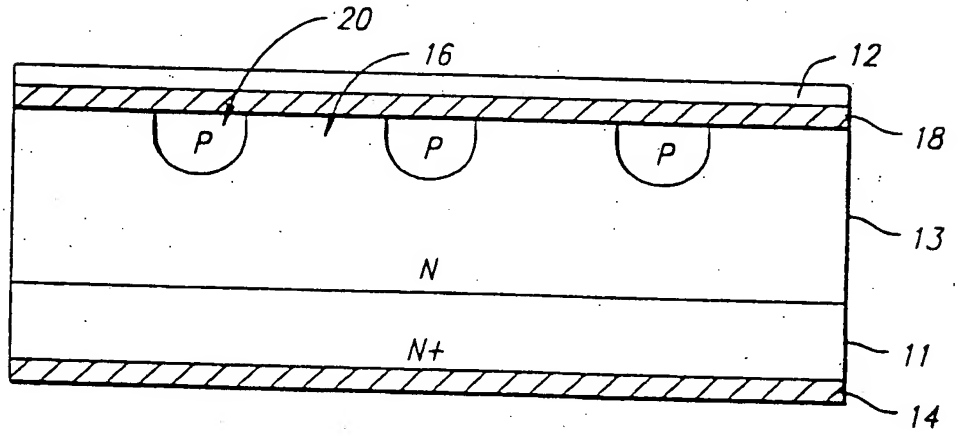


FIG. 1B

FIG. 1C

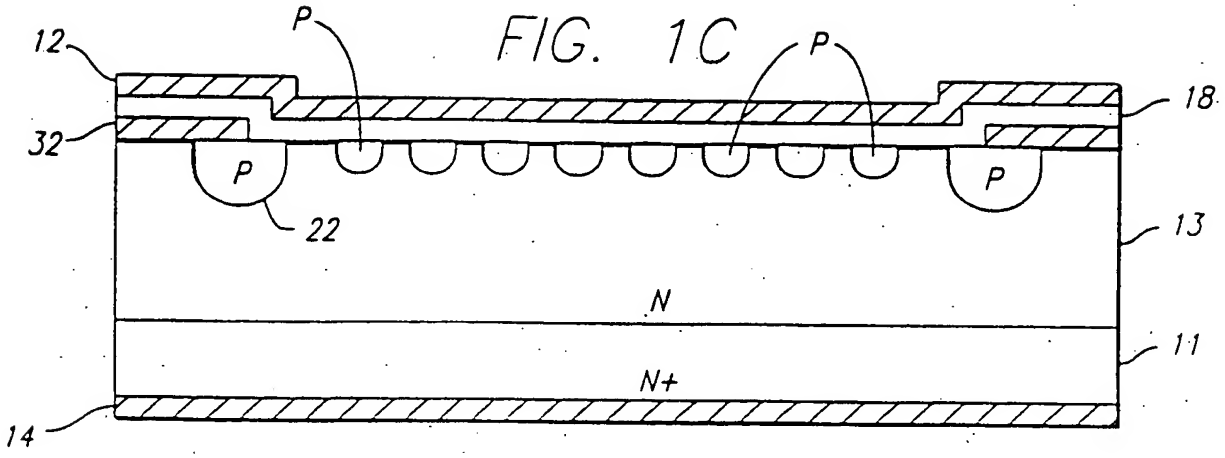


FIG. 2A

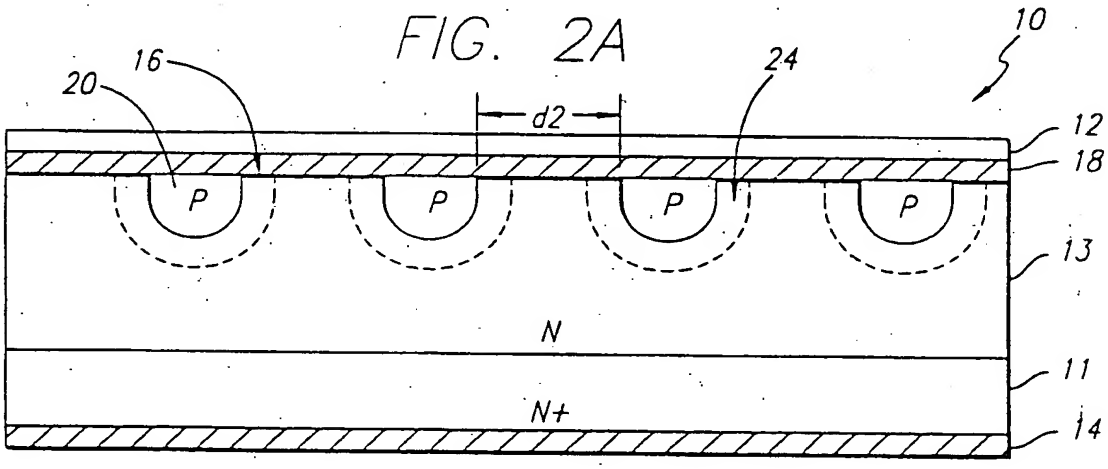


FIG. 2B

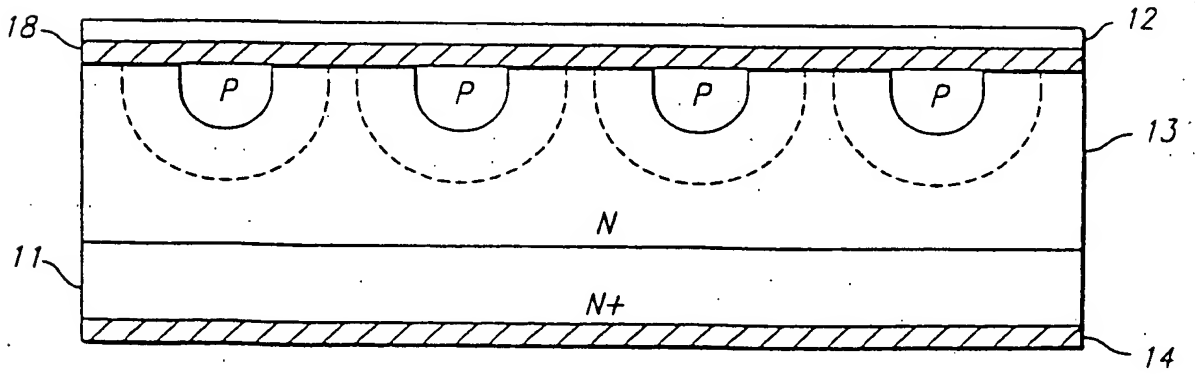


FIG. 2C

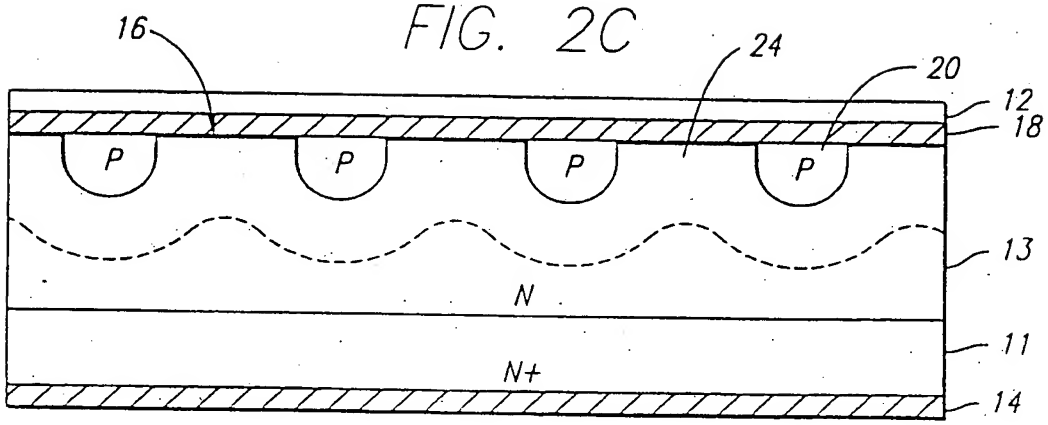


FIG. 3A

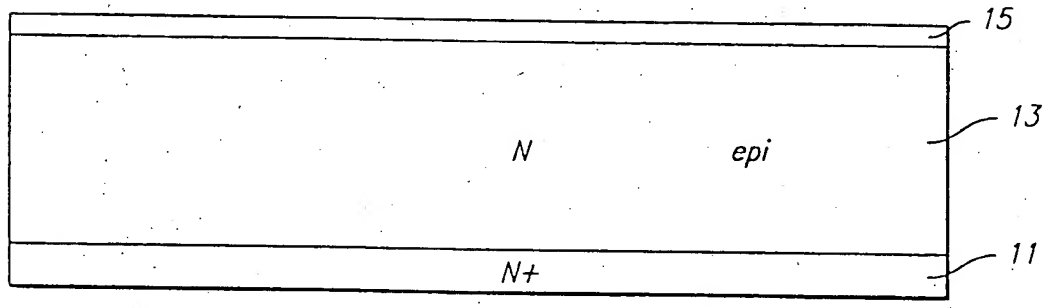


FIG. 3B

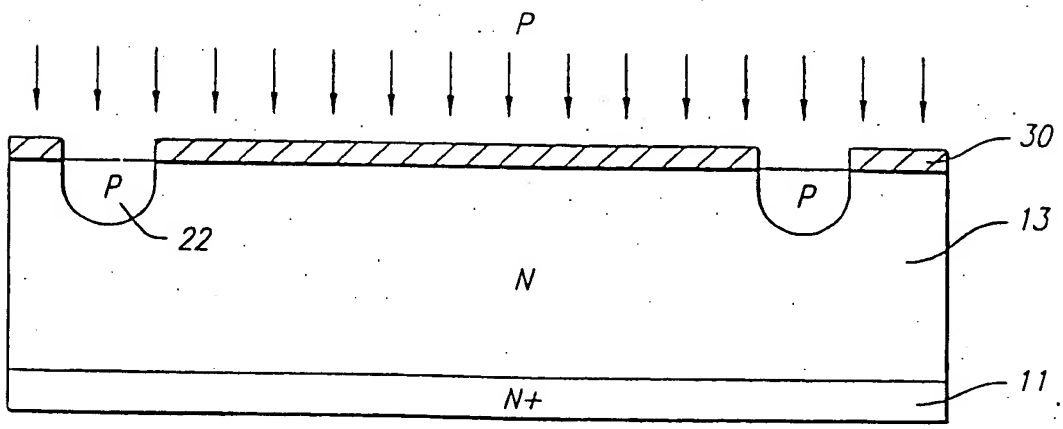


FIG. 3C

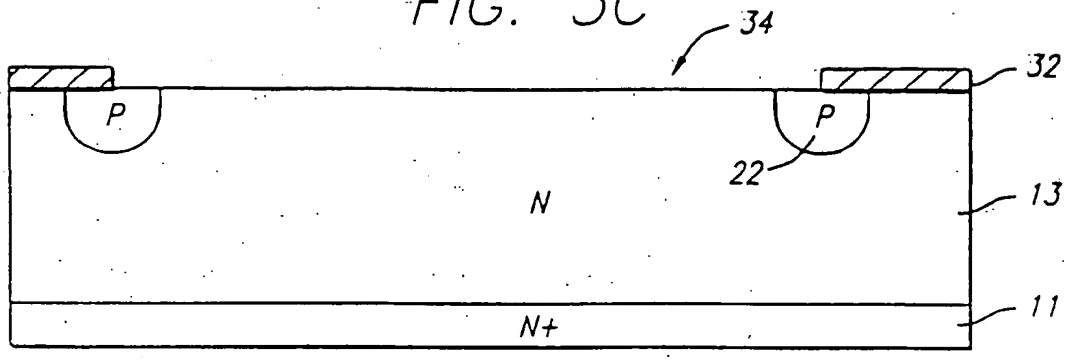


FIG. 3D

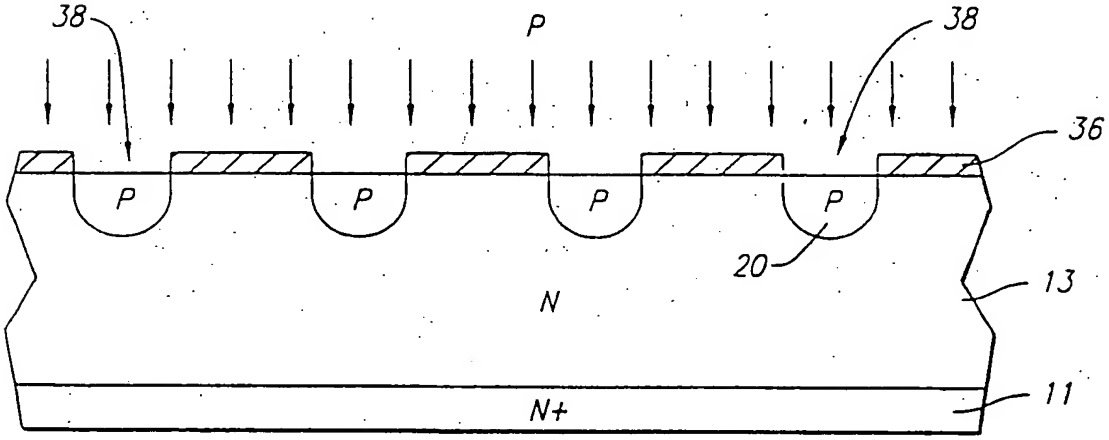


FIG. 3E

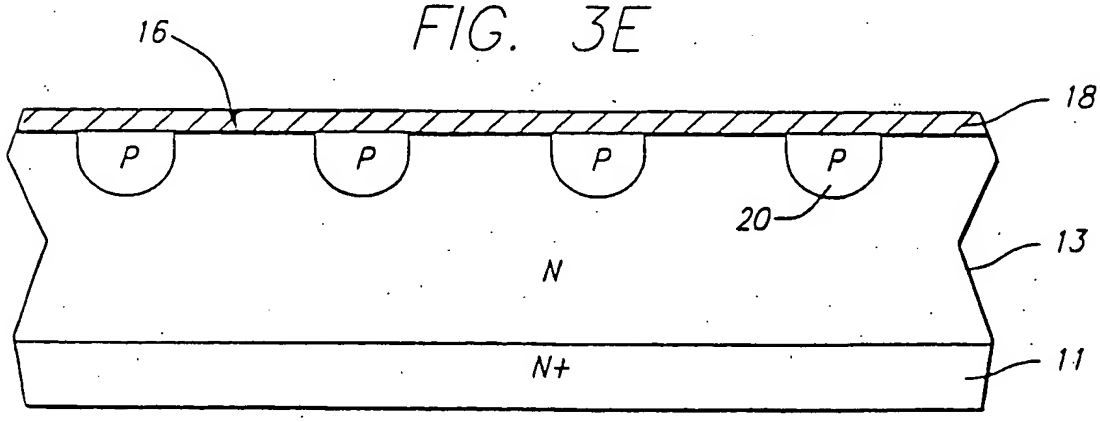


FIG. 3F

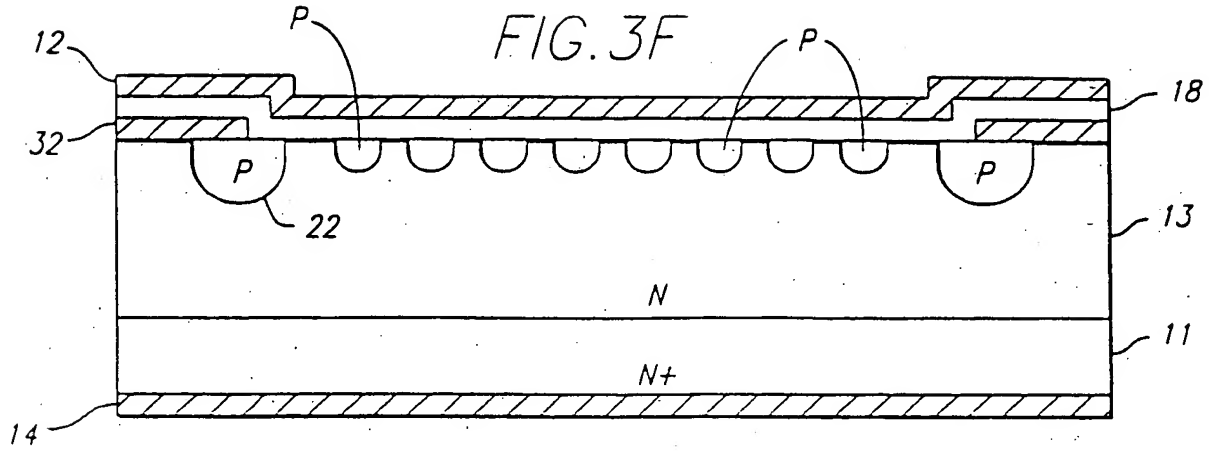
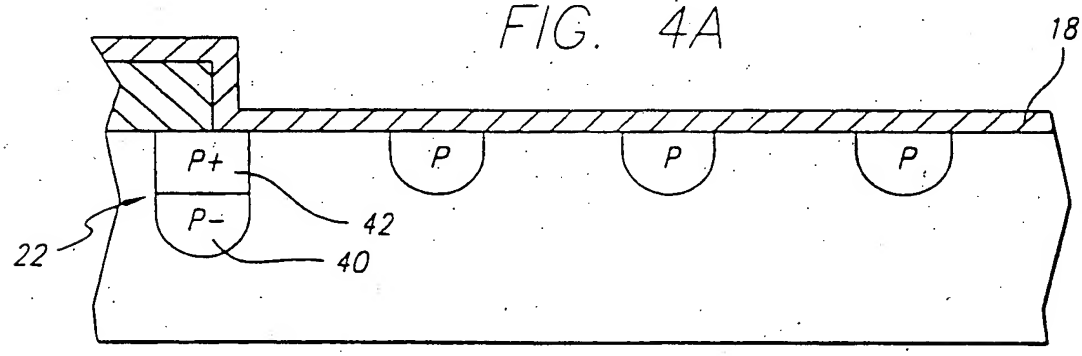


FIG. 4A



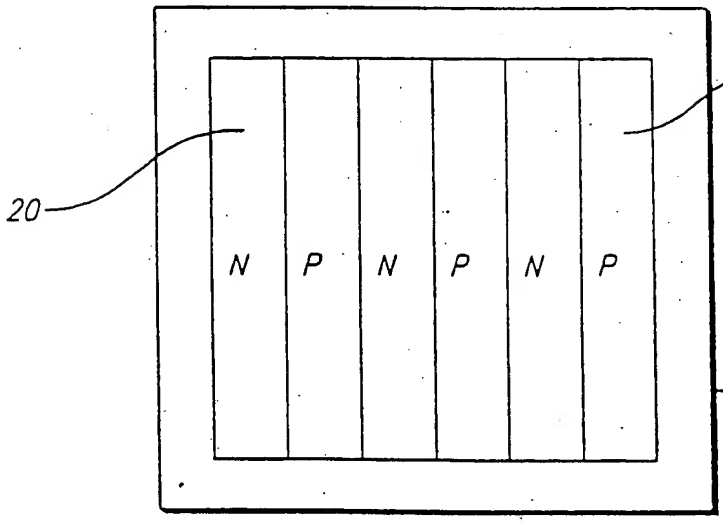


FIG. 4B

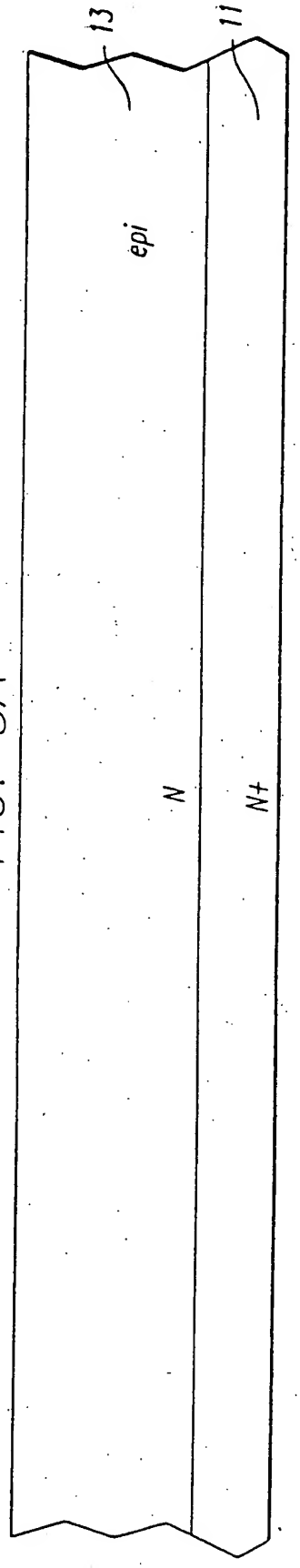


FIG. 5A

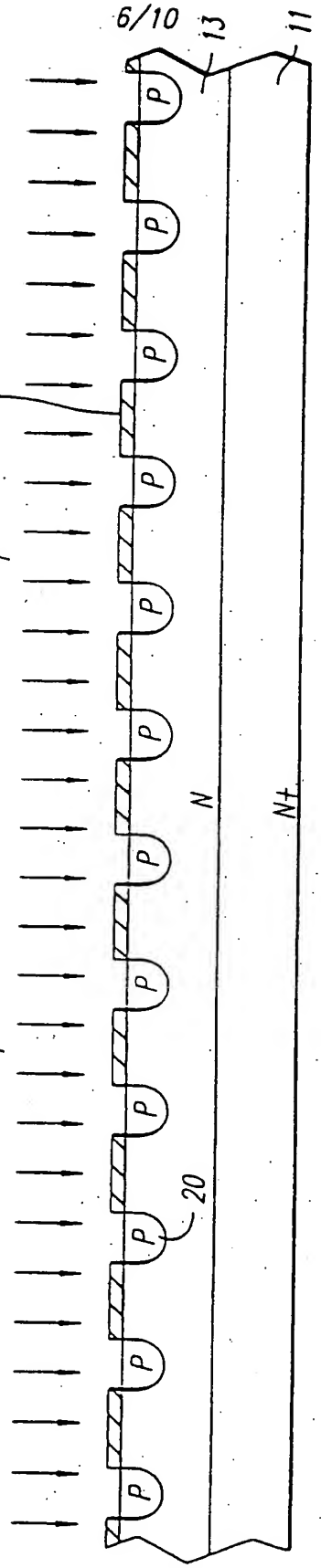


FIG. 5B

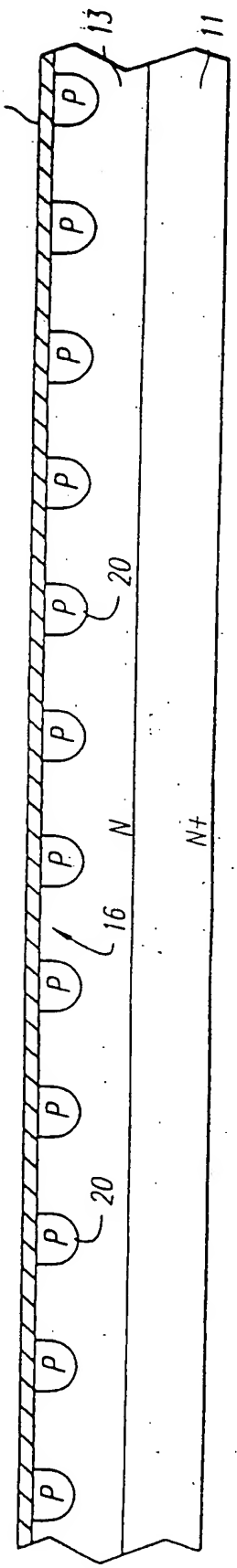


FIG. 5C

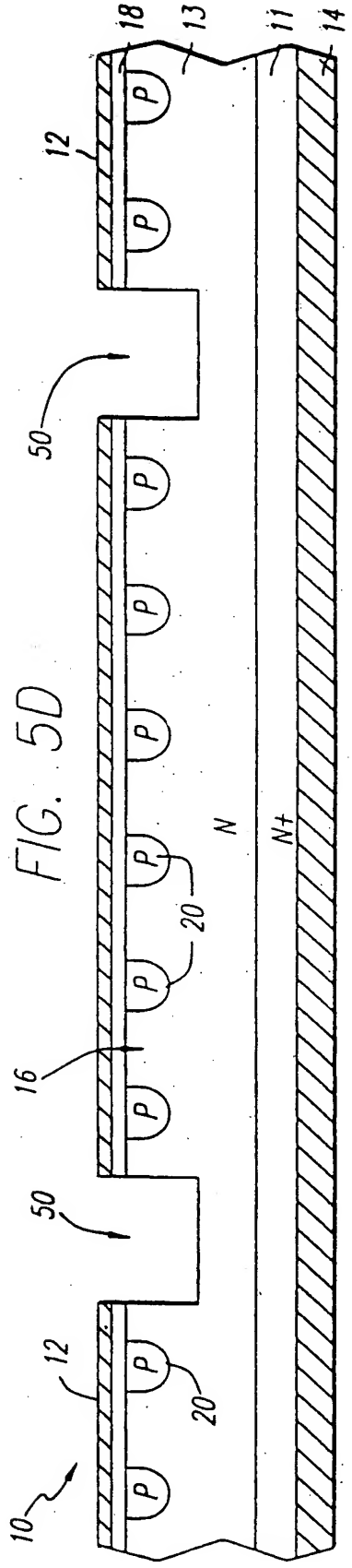


FIG. 5D

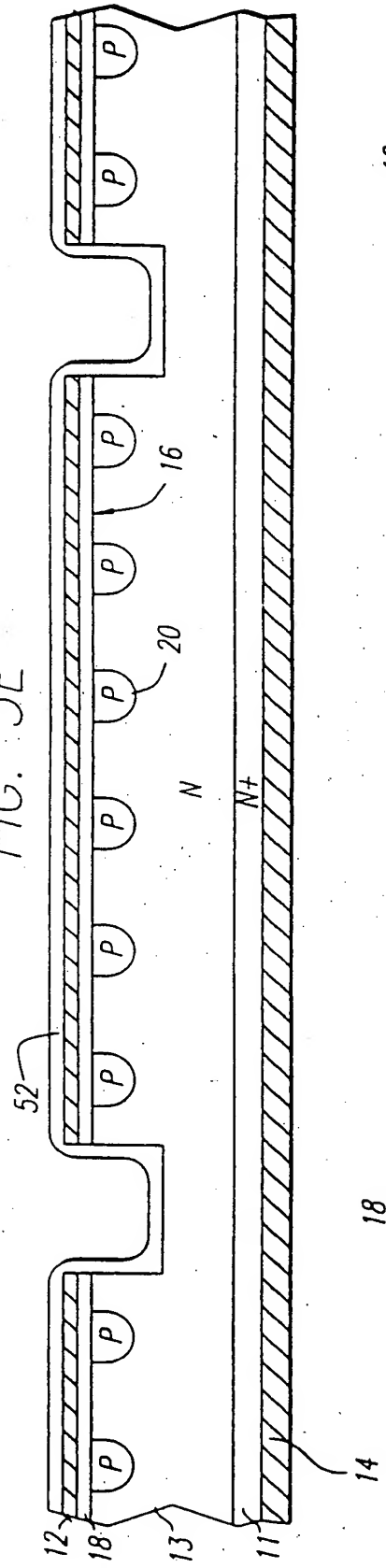


FIG. 5E

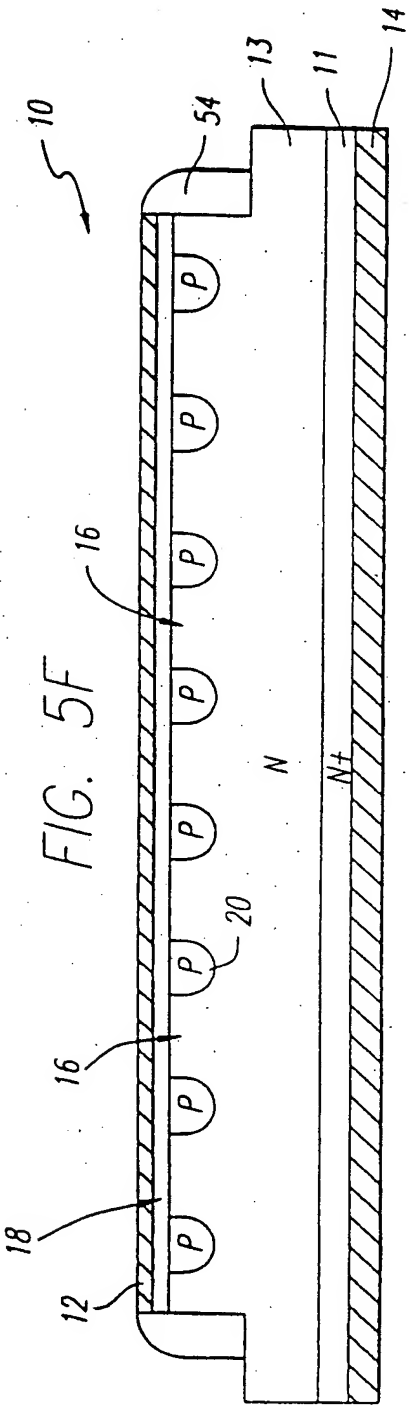


FIG. 5F

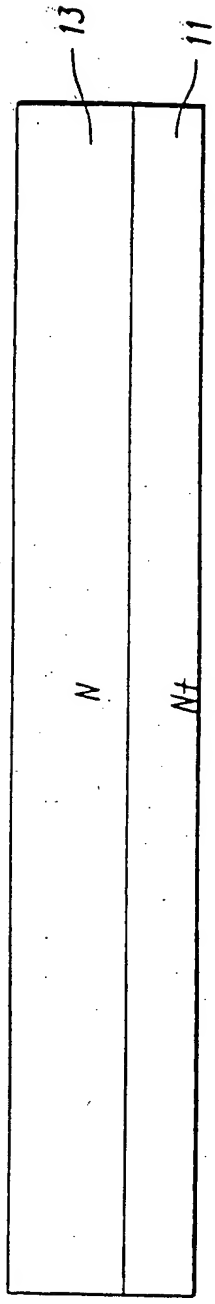


FIG. 6A

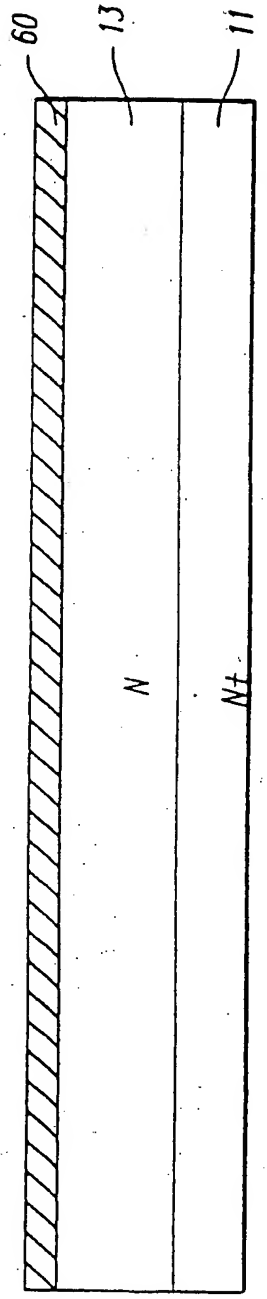


FIG. 6B

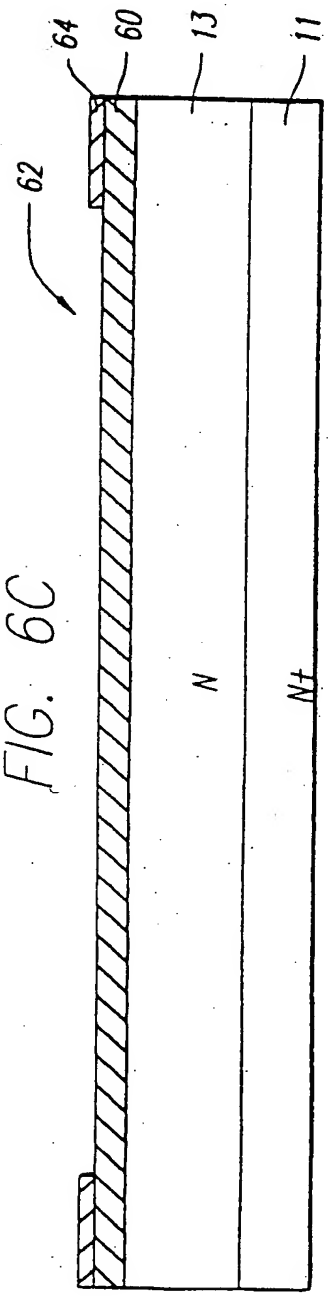


FIG. 6C

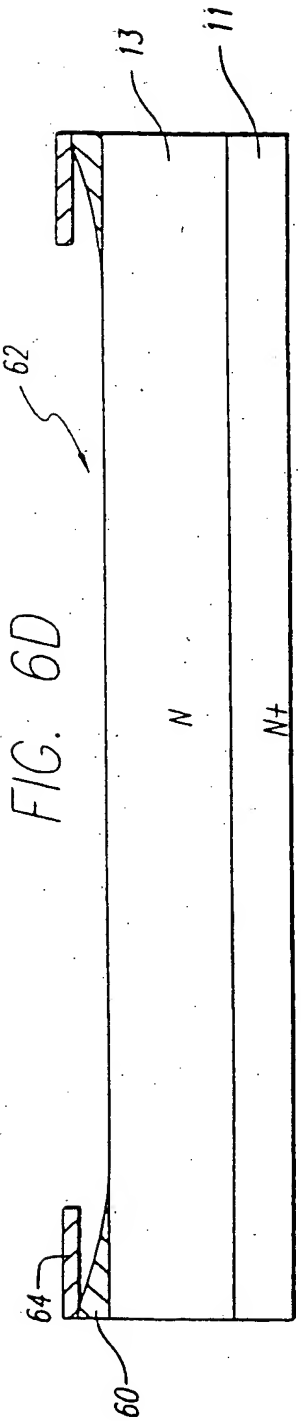


FIG. 6D

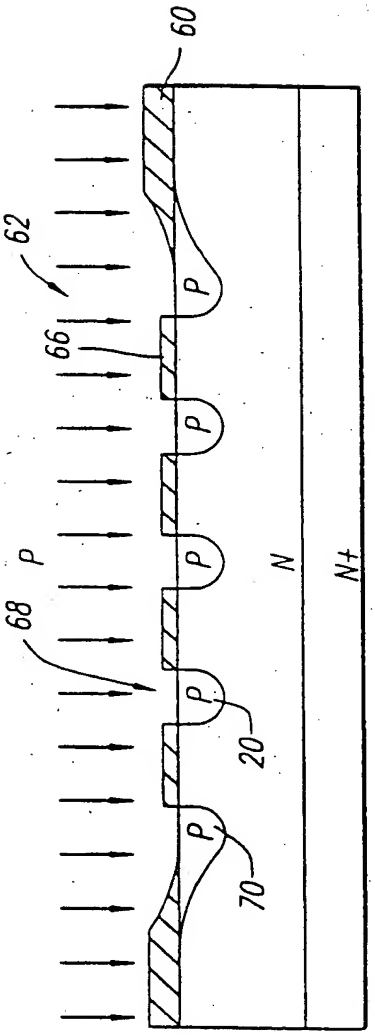


FIG. 6E

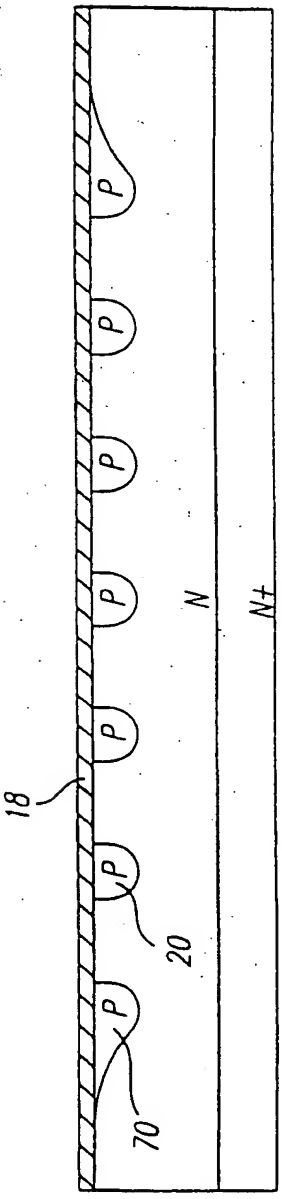
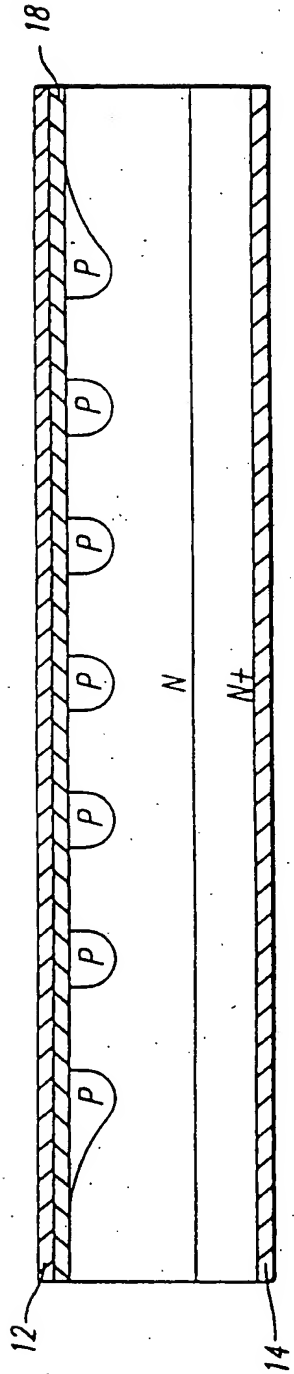


FIG. 6F

FIG. 6G



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/14094

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : H01L 21/338
US CL : 438/167

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : Please See Continuation Sheet

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 5,017,976 A (Sugita) 21 May 1991 (21.05.91), figs. fig. 5, col. 6, lines 47-55	1, 2, 3, 7, 10, 11, 13, 14, 15, 18, 19 --- 6, 8, 16, 17, 20, 21, 22, 23,
Y	US 5,445,978 A (Yilmaz) 29 August 1995 (29.08.95), fig. 10, col. 7, lines 1-26	6, 8, 16, 17
Y, P	US 5,960,286 A (Minami et al.) 28 September 1999 (28.09.1999), fig. 3, col. 5, lines 31-48, col. 1, lines 12-61	20
Y, P	US 5,994,754 A (Hayashi et al.) 30 November 1999 (30.11.99), fig. 1, col. 4, line 66 - col. 5, line 18, col. 2, line 50 - col. 3, line 8	21
Y	US 5,278,443 A (Mori et al.) 11 January 1994 (11.01.94), figs. 4A, 6A, col. 7, line 47 - col. 8, line 12, col. 1, line 20 - col. 2, line 13	22
Y	US 3,649,890 A (Howell et al.) 14 Mar 1972 (14.03.72), col. 1, lines 46-76	23

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search
07 July 2000 (07.07.2000)

Date of mailing of the international search report
25 AUG 2000

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Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US00/14094

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING

Continuation of B. FIELDS SEARCHED Item 1: 438/571, 257/477, 257/484, 257/486

Continuation of B. FIELDS SEARCHED Item 3: (SHOTTKY AND DIODE) AND (GUARD) OR ((SHOTTKY AND DIODE))AND (BLOCKING) OR (SHOTTKY AND DIODE) AND (DEPLETION) OR (SHOCKLEY AND DIODE) AND (BLOCKING)